REMARKS

Claims 1-21 are pending in the present application.

This Amendment is in response to the Office Action mailed April 29, 2002. In the Office Action, the Examiner objected to the drawings and rejected claim 8 under 35 U.S.C. §112; claims 1, 4-5, 8 and 15 under 35 U.S.C. §102(e); and claims 2-3, 9-12 and 16-19 under 35 U.S.C. §103(a). Applicants have amended claims 1-3, 8-10, 12, 15-17, and 19. Reconsideration in light of the amendments and remarks made herein is respectfully requested.

I. DRAWINGS

In the Office Action, the Examiner objected to Figure 2. In particular, the Examiner stated that it is not clear if the system includes a cache. In response, Applicants have amended Figure 2 to change "cache queue" to "data queue" and "cache controller" to "queue controller". A separate letter regarding these proposed changes is being sent to the draftsperson as set forth in MPEP 602.02(r).

Applicants respectfully request acceptance of the amended figure because no substantive new matter has been added. Applicants respectfully request postponement in submitting the formal drawings until the pending claims have been allowed.

II. SPECIFICATION

To keep the terminology in the specification consistent with the drawings, Applicants have also amended the specification with the above terminology changes.

III. REJECTION UNDER 35 U.S.C. §112

In the Office Action, the Examiner rejected claim 8 under 35 U.S.C. §112, second paragraph, due to insufficient antecedent basis. Applicants have amended claim 8 to correct the antecedent basis.

IV. REJECTION UNDER 35 U.S.C. §102(E)

In the Office Action, the Examiner rejected claims 1, 4-5, 8 and 15 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6216208 issued to Greiner et al. ("Greiner"). Applicants respectfully traverse the rejection for the following reasons.

Greiner discloses a prefetch queue responsive to read request sequences. A processor includes a bus sequencing unit (BSU) and a core. An external bus interconnects the processor with other components such as memories (Greiner, col. 2, lines 10-16). The BSU includes an internal cache memory, an internal queue, and a prefetch queue (Greiner, col. 2, lines 17-19). The internal queue monitors requests and informs the prefetch queue of read requests (Greiner, col. 2, lines 61-63). The prefetch queue includes an address buffer to store addresses associated with previous read requests (Greiner, col. 3, lines 28-31). The objective is to determine if the read requests exhibit a pattern indicating that the core is reading from sequential locations in external memory (Greiner, col. 3, lines 1-4).

Greiner does not disclose, either expressly or inherently, a prefetcher to prefetch data from a memory to a data queue and a queue controller to deliver the perfetched data from the data queue to a bus independently of the memory. As clearly shown in Figure 2, the prefetch queue receives the address information from the internal queue, not from a memory. Furthermore, the element 162 is an address buffer to store addresses associated with the request, not the data (Greiner, col. 3, lines 28-31).

To anticipate a claim, the reference must teach every element of a the claim. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Vergegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ...claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). Since the Examiner failed to show that Greiner teaches or discloses any one of the above elements, the rejection under 35 U.S.C. §102 is improper.

Therefore, Applicants believe that independent claims 1, 8 and 15 and their respective dependent claims are distinguishable over the cited prior art references. Accordingly, Applicants respectfully request the rejection under 35 U.S.C. §102(e) be withdrawn.

V. REJECTION UNDER 35 U.S.C. §103(A)

In the Office Action, the Examiner rejected claims 2-3, 9-12 and 16-19 under 35 U.S.C. §103(a) as being unpatentable over Greiner in view of U.S. Patent No. 6356962 issued to Kasper et al. ("Kasper"). Applicants respectfully traverse the rejection for the following reasons.

Greiner discloses a discloses a prefetch queue responsive to read request sequences. Greiner, as discussed above, does not disclose a prefetcher to prefetch data from a memory to a data queue.

Kasper discloses a network device and method of controlling flow of data arranged in frames in a data-based network. A look-ahead watermark functions as a synchronizing signal in a FIFO memory structure to indicate that sufficient storage exists to receive more bursts (Kasper, col. 3, lines 35-39).

Here, there is no motivation to combine Greiner and Kasper because neither of them addresses the problem of reducing memory access latencies from a bus. There is no teaching or suggestion that a prefetcher to prefetch data from a memory to a data queue is present. Greiner and Kasper, read as a whole, does not suggest the desirability of prefetching data from a memory to a data queue and delivering the prefetched data to a bus independently of the memory. For the above reasons, the rejection under 35 U.S.C. §103(a) is improperly made.

The Examiner failed to establish a prima facie case of obviousness and failed to show there is teaching, suggestion or motivation to combine the references. "When determining the patentability of a claimed invention which combined two known elements, 'the question is whether there is something in the prior art as a whole suggest the desirability, and thus the obviousness, of making the combination.'" In re Beattie, Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 1462, 221 U.S.P.Q. (BNA) 481, 488 (Fed. Cir. 1984). To defeat patentability based on obviousness, the suggestion to make the new product having the claimed characteristics must come from the prior art, not from the hindsight knowledge of the invention. Interconnect Planning Corp. v. Feil, 744 F.2d 1132, 1143, 227 U.S.P.Q. (BNA) 543, 551 (Fed. Cir. 1985). To prevent the use of hindsight based on the invention to defeat patentability of the invention, this court requires the Examiner to show a motivation to combine the references that create the case of obviousness. In other words, the Examiner must show reasons that a skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the prior elements from

the cited prior references for combination in the manner claimed. In re ROUFFET, 149 F.3d 1350 (Fed. Cir. 1996), 47 U.S.P.Q.2d (BNA) 1453. "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or implicitly suggest the claimed invention or the Examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." Ex parte Clapp, 227 USPQ 972, 973. (Bd.Pat.App.&Inter. 1985).

Therefore, Applicants believe that independent claims 1, 8 and 15 and their respective dependent claims are distinguishable over the cited prior art references. Accordingly, Applicants respectfully request the rejections under 35 U.S.C. §112, 35 U.S.C. §102(e), and 35 U.S.C. §103(a) be withdrawn.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

1. The paragraph beginning on page 2, line 2; has been amended as follows:

-- The present invention is a method and apparatus to reduce latency in accessing a memory from a bus. The apparatus comprises a pre-fetcher and a ~~cache~~ queue controller. The pre-fetcher pre-fetches a plurality of data from the memory to a ~~cache~~ data queue in response to a request. The ~~cache~~ queue controller is coupled to the ~~cache~~ data queue and the pre-fetcher to deliver the pre-fetched data from the ~~cache~~ data queue to the bus in a pipeline chain independently of the memory.--

2. The paragraph beginning on page 5, line 23; has been amended as follows:

-- Caching and pre-fetching reduce the initial latency and subsequent latency. After a bus-to-memory read stream is completed, the pre-fetched data are kept in a read ~~cache~~ data queue. If the consecutive bus-to-memory read is a follow-on to the initial read, the read cycle continues from where the initial read left off. For subsequent data transfers, a watermark level is determined by calculating the amount of data that could have been transferred during the latency time on the bus interface. This is the amount of data that needs to be pre-fetched to keep a continuous data transfer stream. By delivering data continuously from the local ~~cache~~ data queue independently of the memory, latency due to subsequent data transfers is reduced.--

3. The sentence beginning on page 7, line 16; has been amended as follows:

-- The bus access circuit 125 includes a peripheral bus controller 210, a pre-fetcher 215, a ~~cache~~ queue controller 230, a data coherence controller 250, a scheduler 260, a data mover 270, and a ~~cache~~ data queue 280.--

4. The paragraph beginning on page 7, line 23; has been amended as follows:

-- The peripheral bus controller (PBC) 210 receives control and request signals from the peripheral bus and interfaces to the pre-fetcher 215 and the ~~cache~~ queue controller ~~(CC)~~ (QC) 230. The PBC 210 decodes the access request and determines if the access request is valid. If the access request is valid, the PBC 210 forwards the access request to the RPG 220 and to the ~~(CC)~~ (QC) 230. The ~~(CC)~~ (QC) 230 determines if there is a hit or a miss. The hit/miss detector can be performed by comparing the address of the request with the address range of the ~~cache~~ data queue. The RPG 220 returns a control signal to the PBC 210 for moving data from the cache queue 280 to the peripheral bus. Upon receipt of the control signal from the RPG 220, the PBC 210 sends a command to the ~~(CC)~~ (QC) 230 to start the data transfer from the ~~cache~~ data queue 280 to the peripheral bus.--

5. The sentence beginning on page 8, line 13; has been amended as follows:

--The watermark monitor 225 determines if the amount of data in the ~~cache~~ data queue 280 is above a pre-determined level.--

6. The sentence beginning on page 8, line 17; has been amended as follows:

--If the request results in a hit, (e.g., the requested data item is in the ~~cache~~ data queue 280), the RPG 220 sends a control signal to the PBC 210 to enable the PBC 210 to start data transfer from the ~~cache~~ data queue 280.--

7. The paragraph beginning on page 9, line 5; has been amended as follows:

-- The ~~cache~~ queue controller ~~(CC)~~ (QC) 230 receives control information from the PBC 210 and interacts with the watermark monitor 225, the data mover 270, and the cache queue 280. The ~~(CC)~~ (QC) 230 manages the data allocation for the ~~cache~~ data queue 280 by monitoring the amount of data in the ~~cache~~ data 280. This information is forwarded to the data mover 270 for controlling data movement from the memory to the ~~cache~~ data queue 280. The ~~(CC)~~ (QC) 230 also controls the data movement from the ~~cache~~ data queue 280 to the peripheral bus by responding to the status information provided by the PBC 210.--

8. The paragraph beginning on page 9, line 21; has been amended as follows:

-- The data coherence controller (DCC) 250 receives a control signal, (e.g., a clear data signal), from the RPG 220 and forward to the data mover 270, which in ~~turns forward~~ turn forwards to the ~~(CC)~~ (QC) 230. The ~~(CC)~~ (QC) 230 performs a data purge operation upon receiving this clear data signal.--

9. The paragraph beginning on page 10, line 18; has been amended as follows:

-- The ~~cache~~ data queue ~~(CQ)~~ (DQ) 280 stores data items from the memory as transferred by the DM 270. The amount of data in the ~~(CQ)~~ (DQ) 280 is monitored by the ~~CC~~ QC 230. The data items stored in the ~~(CQ)~~ (DQ) 280 are read out to the peripheral bus when the ~~CC~~ QC 230 determines that there is a hit upon receiving a read request from the bus as generated by the PBC 210, or when the missed data are transferred from the memory to the ~~(CQ)~~ (DQ) 280.--

10. The paragraph beginning on page 10, line 24; has been amended as follows:

-- Activities in the bus access circuit 125 includes bus decode by the PBC 210, cache check by the ~~CC~~ QC 230, request generation by the RPG 220, data move and purging by the scheduler 260 and the DM 270, and data delivery and caching by the ~~CC~~ QC 230 and the ~~(CQ)~~ (DQ) 280. These activities can be illustrated in a timing diagram for a particular access request.--

11. The sentence beginning on page 17, line 22; has been amended as follows:

--Next, the process 650 stores the read data in the read ~~cache~~ data queue (Block 870) and is then terminated.--

IN THE CLAIMS

The following is a set of claims showing all amended claims.

1. (TWICE AMENDED) A method comprising:

pre-fetching a plurality of data from a memory to a ~~cache~~ data queue in response to a request; and

delivering the pre-fetched data from the ~~cache~~ data queue to a bus independently of the memory.

2. (AMENDED) The method of claim 1 wherein pre-fetching comprises:

determining if an amount of data in the ~~cache~~ data queue is above a predetermined level; and

placing the request to a memory controller controlling the memory if the amount of data is not above the predetermined level, the request causing the memory controller to transfer the plurality of data to the ~~cache~~ data queue, the request being buffered in a request queue.

3. (AMENDED) The method of claim 2 wherein the delivering comprises:

transferring the data from the ~~cache~~ data queue to the bus if the data in the ~~cache~~ data queue is ready.

8. (TWICE AMENDED) An apparatus comprising:

a pre-fetcher to pre-fetch a plurality of data from a memory to a ~~cache~~ data queue in response to a request; and

a ~~cache~~ queue controller coupled to the ~~cache~~ data queue and the pre-fetcher to deliver the pre-fetched data from the ~~cache~~ data queue to ~~the~~ a bus independently of the memory.

9. (AMENDED) The apparatus of claim 8 wherein the pre-fetcher comprises:

a watermark monitor to determine if an amount of data in the ~~cache~~ data queue is above a predetermined level;

a request packet generator coupled to the watermark monitor to place the request to a memory controller controlling the memory if the amount of data is not above the predetermined

level, the request causing the memory controller to transfer the plurality of data to the ~~cache~~ data queue; and

a request queue coupled to the request packet generator to store the request provided by the request packet generator.

10. (AMENDED) The apparatus of claim 9 wherein the ~~cache~~ queue controller transfers the data from the ~~cache~~ data queue to the bus if the data in the ~~cache~~ data queue is ready.

12. (AMENDED) The apparatus of claim 11 further comprising:

a data mover coupled to the ~~cache~~ data queue and the scheduler to transfer data from the memory to the ~~cache~~ data queue, the data mover purging data corresponding to a marked entry from the scheduler.

15. (TWICE AMENDED) A system comprising:

a memory;

a bus; and

a bus access circuit coupled to the memory and the bus to reduce latency in accessing the memory from the bus, the bus access circuit including:

a pre-fetcher to pre-fetch a plurality of data from the memory to a ~~cache~~ data queue in response to a request, and

a ~~cache~~ queue controller coupled to the ~~cache~~ data queue and the pre-fetcher to deliver the pre-fetched data from the ~~cache~~ data queue to the bus independently of the memory.

16. (TWICE AMENDED) The system of claim 15 wherein the pre-fetcher comprises:

a watermark monitor to determine if an amount of data in the ~~cache~~ data queue is above a predetermined level;

a request packet generator coupled to the watermark monitor to place the request to a memory controller controlling the memory if the amount of data is not above the predetermined

level, the request causing the memory controller to transfer the plurality of data to the ~~cache~~ data queue; and

a request queue coupled to the request packet generator to store the request provided by the request packet generator.

17. (AMENDED) The system of claim 16 wherein the ~~cache~~ queue controller transfers the data from the ~~cache~~ data queue to the bus if the data in the ~~cache~~ data queue is ready.

19. (AMENDED) The system of claim 18 wherein the bus access circuit further comprising:

a data mover coupled to the ~~cache~~ data queue and the scheduler to transfer data from the memory to the ~~cache~~ data queue, the data mover purging data corresponding to a marked entry from the scheduler.

CONCLUSION

In view of the amendments and remarks made above, it is respectfully submitted that the pending claims are in condition for allowance, and such action is respectfully solicited.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on: July 24, 2002.

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